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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,730	08/21/2003	Shinsaku Sekido	60188-630	6195

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EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,730	SEKIDO ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 August 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2.0 Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. (USPG_PUB No. 2005/0132306), in view of Yonezawa et al. (U.S. Patent No. 6,795,802).

2.1 In considering the independent claim 1, Smith et al. substantially teaches a circuit simulation method comprising the steps of (a) recognizing, from mask layout data for an integrated circuit, the shape of an electronic device to be

analyzed which is provided in the integrated circuit, and obtaining data concerning the size of the electronic device to be analyzed *(fig.7-14, 16-25, also pg.13-18 (0299-0359)*; (b) determining the electrical characteristic of an electronic device for measurement, and measuring the size of each portion of the electronic device for measurement, as well as items each serving as an index of a stress applied to the electronic device to be analyzed *(fig.7-14, 16-25, also pg.13-18 (0299-0359)*; (c) extracting, based on at least the size of each portion of the electronic device for measurement, parameters from data concerning the electrical characteristic of the electronic device for measurement which has been determined in the step (b) *(fig.7-14, 16-25, item #31; also pg.13-18 (0299-0359)*; and (d) utilizing a circuit simulator to select, from among the extracted parameters, a parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit, and to perform circuit simulation in consideration of a stress applied to each electronic device to be analyzed *(fig.7-14, 16-25, also pg.13-18 (0299-0359)*. Smith et al. does not clearly teach applied stress to the device. Yonezawa et al. teaches applied stress and further teaches a stress calculation unit *(fig.5 (111b), col.7 line 43-col.10 line 65; also col.12 line 61-col.14 line 49)*. It would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the stress calculation of Yonezawa et al. in the circuit simulation method of Smith et al. for the purpose of calculating and analyzing the stress applied to the device. Yonezawa et al. further teaches the improvement of processing efficiency *(col.12 lines 25-45)*.

2.2 With regards to claim 2, the combined teachings of Smith et al and Yonezawa et al. substantially teach the step (b), at least an item serving as an index of a stress applied from an isolation insulating film to the electronic device to be analyzed is measured, and wherein in the step (d), the circuit simulation is performed in consideration of the stress applied from the isolation insulating film to the electronic device to be analyzed *(see Yonezawa et al. fig.1-5, 12 & their description and Smith et al. 7-16,25).*

2.3 As per claim 3, the combined teachings of Smith et al and Yonezawa et al. substantially teach in the step (c), a plurality of parameters are extracted for each of the equal-sized electronic devices to be analyzed, based on the items each serving as an index of a stress applied to the electronic device to be analyzed (*see Smith et al. (fig.7-14, 16-25, item #31; also pg.13-18 (0299-0359); also Yonezawa et al. fig.1-5, 12 & their description).*

2.4 Regarding claim 4, the combined teachings of Smith et al and Yonezawa et al. substantially teach the step of inputting an additional model to the circuit simulator, the additional model being prepared based on measurement data that has been obtained in the step (b) and that serves as an index of a stress, and wherein in the step (d), a correction is made using the additional model when selecting a parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit *(see Smith et al. fig.7-16, 25 & their description also pg.13-18 (0299-0359); also Yonezawa et al. fig.1-5, 12 & their description).*

2.5 With regards to claim 5, the combined teachings of Smith et al and Yonezawa et al. substantially teach the step of preparing a reference table including pieces of information for associating each electronic device to be analyzed, which is provided in the integrated circuit, with the parameter that should be assigned to the electronic device to be analyzed, and the step of inputting the reference table to the circuit simulator, the reference table being prepared based on the items each serving as an index of a stress applied to the electronic device to be analyzed, and wherein in the step (d), the selection of the parameter suitable for each electronic device to be analyzed which is provided in the integrated circuit is automatically carried out using the reference table *(see Smith et al. fig.7-17,20-25(item 34-1 of fig.7) & their description; also pg.13-18 (0299-0359); also Yonezawa et al. fig.1-5,12 & their description).*

2.6 As per claim 6, the combined teachings of Smith et al and Yonezawa et al. substantially teach that the reference table is used to associate each electronic device to be analyzed, which is provided in the integrated circuit, with a plurality of weighted parameters (*see Smith et al. fig.7-17, 20-25& their description; also pg.17-18 (0339-0359); also Yonezawa et al. fig.1-5, 12 & their description).*

2.7 Regarding claim 7, the combined teachings of Smith et al and Yonezawa et al. substantially teach the electronic device to be analyzed and the electronic device for measurement are each formed by a MIS transistor or a bipolar transistor (*see Smith et al. fig.7-17, 20-25& their description; also pg.12-18 (00294-0359); also Yonezawa et al. fig.1-5, 12 & their description).*

2.8 With regards to claim 8, the combined teachings of Smith et al and Yonezawa et al. substantially teach wherein the electronic device to be analyzed and the electronic device for measurement are each formed by a MIS transistor comprising a gate electrode, a gate insulating film, an active region and an isolation insulating film surrounding the active region, and *wherein the items*, each serving as an index of a stress applied to the electronic device to be analyzed, include at least one of the position of the gate electrode in the active region, the size of the active region, and the width of the isolation insulating film (*see Smith et al. fig.7-17, 20-25, 42 & their description; also pg.12-18 (00294-0359); also Yonezawa et al. fig.1-5, 12 & their description).*

2.9 As per claim 9, the combined teachings of Smith et al and Yonezawa et al. substantially teach wherein the items, each serving as an index of a stress applied to the electronic device to be analyzed, further include at least one of the depth of the active region, a method for forming the isolation insulating film, the depth of the isolation insulating film, a material for use in forming the isolation insulating film, the size of the gate insulating film, and a material for use in forming the gate insulating film (*see Smith et al. fig.7-17, 20-25, 42 & their description; also para (0467, 0539.0579, 0752) and 0009-0037; also pg.12-18 (00294-0359); also Yonezawa et al. fig.1-5, 12 & their description).*

2.10 Regarding claim 10, the combined teachings of Smith et al and Yonezawa et al. substantially teach in the step (d), the circuit simulation is performed in consideration of a stress applied from the gate insulating film to the

electronic device to be analyzed *(fig.7-14, 16-25, also pg.13-18 (0299-0359); also Yonezawa et al. fig.1-5, 12 & their description).*

2.11 As per claim 11, the combined teachings of Smith et al and Yonezawa et al. substantially teach in the step (b), at least an item that serves as an index of a stress applied from an interlayer dielectric film to the electronic device to be analyzed is measured, and wherein in the step (d), the circuit simulation is performed in consideration of the stress applied from the interlayer dielectric film to the electronic device to be analyzed *(see Yonezawa et al. fig.1-5, 12 & their description and Smith et al. 7-16,25 & their description).*

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

3.1 Venugopal et al. (USPG_PUB No. 2002/0152447) teaches an integrated circuit design error detector for electrostatic discharge and latch-up applications.

3.2 Toda (U.S. Patent No. 6,144,931) teaches a wafer expansion and contraction simulation method.

3.3 White et al. (USPG_PUB No. 203/0237064) teaches a characterization and verification for integrate circuits designs.

3.4 Smith et al. (USPG_PUB No. 2003/0229875) teaches the use of models in integrated circuit fabrication.

4. Claims 1-11 are rejected and this action is non-final. Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 19, 2006

APL

Paul L. Rodriguez 5/6/06
Primary Examiner
Art Unit 2125 2123